IN THE CLAIMS

1. (Original) A method comprising:

computing an energy delay^2 product metric for a current architecture configuration over a predetermined period of time;

comparing the computed energy delay^2 product metric to an energy delay^2 product metric of a prior architecture configuration to determine an energy effectiveness of the current architecture configuration; and

adjusting a number of active instruction schedulers of the current architecture configuration according to the energy effectiveness of the current architecture configuration.

2. (Original) The method of claim 1, wherein computing the energy delay^2 product metric comprises:

selecting an active instruction scheduler from one or more active instruction schedulers of the current architecture configuration matching a selected instruction scheduler type;

computing an energy consumption value for the selected instruction scheduler and one or more associated logic elements as a product of an access count and a predetermined energy per access amount of the selected instruction scheduler and the predetermined period of the time squared;

repeating selecting of the instruction scheduler, computing of the energy consumption value and storing of the energy consumption value for each instruction scheduler of the current architecture configuration matching the selected instruction scheduler type to form an energy consumption sum;

storing the energy consumption product sum for the instruction selected scheduler type; and

repeating the selecting the active instruction scheduler, computing of the energy consumption product, repeating, and storing the energy consumption product for each instruction scheduler type of the current architecture configuration to form the energy consumption value of the current architecture configuration.

3. (Original) The method of claim 1, wherein comparing the computed energy delay^2 product value comprises:

selecting an instruction scheduler type of the current architecture configuration;

determining a computed energy consumption product for the selected instruction scheduler type;

comparing the computed energy delay^2 product of the selected instruction scheduler type to a previously computed energy delay^2 product value;

identifying a decrease in the effectiveness of the current architecture configuration if the computed energy delay^2 product is less than the previously computed energy consumption product; and

identifying an increase in the effectiveness of the current architecture configuration if the computed energy delay^2 product is greater than the previously computed energy delay^2 product.

4. (Original) The method of claim 1, wherein adjusting comprises:

identifying an increase in the effectiveness of the current architecture configuration;

identifying a direction indicator state for an instruction scheduler type of the current architecture configuration as one of an increased state and a decreased state;

increasing the number of active instruction schedulers for the current architecture configuration if the direction indicator is in an increased state;

reducing the number of active instruction schedulers for the current architecture configuration if the direction indicator is in a decreased state; and

maintaining a state of the direction indicator for the selected instruction scheduler type.

5. (Original) The method of claim 1, wherein adjusting comprises:

identifying a decrease in the effectiveness of the current architecture configuration;

identifying a direction indicator state for an instruction scheduler type of the current architecture configuration as one of an increased state and a decreased state;

reducing the number of active instruction schedulers for the current architecture configuration if the direction indicator is in an increased state;

increasing the number of active instruction schedulers for the current architecture configuration if the direction indicator is in a decreased state; and

switching a state of the direction indicator for the selected instruction scheduler type.

6. (Original) The method of claim 5, wherein increasing the number of active instruction schedulers comprises:

selecting a disabled instruction scheduler of the current architecture configuration; and

enabling a clock input to the instruction scheduler and one or more associated functional blocks.

7. (Currently Amended) The method of claim 5, wherein decreasing the number of active instruction schedulers comprises:

selecting an active instruction scheduler of the current architecture configuration; and

disabling a clock input to the instruction scheduler and one or more associated functional units.

8. (Original) The method of claim 1, further comprising:

executing an adjusted architecture configuration over a predetermined interval;

computing an energy delay^2 product for the adjusted architecture configuration consumed during execution over the predetermined interval;

computing an energy delay^2 product for an increased architecture configuration having one or more additional active instruction schedulers than the adjusted configuration architecture consumed during execution over a reduced time interval;

computing an energy delay^2 product consumed by a decreased architecture configuration having a reduced number of active instruction schedulers than the adjusted configuration architecture consumed during over the reduced interval of time;

normalizing the computed energy delay^2 products for the increased and decreased architecture configurations;

identifying an architecture configuration having a lowest energy delay^2 product; and

selecting the identified architecture configuration as a current architecture configuration.

9. (Original) The method of claim 8, further comprising:

detecting one of the increased architecture configuration or decreased architecture configuration as having the lowest energy delay^2 product;

performing the method of claim 8 with the detected architecture configuration as the adjusted architecture configuration.

10. (Original) The method of claim 2, wherein computing the energy consumption value comprises:

calculating an energy consumption value for one or more functional units associated with the selected instruction scheduler;

calculating an energy consumption value for a register file associated with the selected instruction scheduler;

calculating an energy consumption value for each component the selected instruction scheduler;

summing the energy consumption values of the instruction scheduler, functional units and register file; and

computing the energy delay^2 product as a product of the energy consumption sum and a square of the predetermined time interval.

11. (Original) An article of manufacture including a machine readable medium having stored thereon instructions which may be used to program a system to perform a method, comprising:

computing an energy delay^2 product value for a current architecture configuration over a predetermined period of time;

comparing the computed energy delay^2 product value to an energy consumption value of a prior architecture configuration to determine an energy effectiveness of the current architecture configuration; and

adjusting a number of active instruction schedulers of the current architecture configuration according to the energy effectiveness of the current architecture configuration.

12. (Original) The article of manufacture of claim 11, wherein computing the delay^2 product value comprises:

selecting an active instruction scheduler from one or more active instruction schedulers of the current architecture configuration matching a selected instruction scheduler type;

computing an energy consumption value for the selected instruction scheduler and one or more associated logic elements as a product of an access count and a predetermined energy per access amount of the selected instruction scheduler and the predetermined period of the time squared;

repeating selecting of the instruction scheduler, computing of the energy consumption value and storing of the energy consumption value for each instruction scheduler of the current architecture configuration matching the selected instruction scheduler type to form an energy consumption sum;

storing the energy consumption product sum for the instruction selected scheduler type; and

repeating the selecting the active instruction scheduler, computing of the energy consumption value, repeating, and storing the energy consumption value for each instruction scheduler type of the current architecture configuration to form the energy consumption value of the current architecture configuration.

13. (Original) The article of manufacture of claim 11, wherein comparing the computed energy delay^2 product value comprises:

selecting an instruction scheduler type of the current architecture configuration;

determining a computed energy delay^2 product for the selected instruction scheduler type;

comparing the computed energy delay^2 product of the selected instruction scheduler type to a previously computed energy consumption product value;

identifying a decrease in the effectiveness of the current architecture configuration if the computed energy delay^2 product is less than the previously computed energy delay^2 product; and

identifying an increase in the effectiveness of the current architecture configuration if the computed energy delay^2 product is greater than the previously computed energy delay^2 product.

14. (Original) The article of manufacture of claim 11, wherein adjusting comprises:

identifying an increase in the effectiveness of the current architecture configuration;

identifying a direction indicator state for an instruction scheduler type of the current architecture configuration as one of an increased state and a decreased state;

increasing the number of active instruction schedulers for the current architecture configuration if the direction indicator is in an increased state;

reducing the number of active instruction schedulers for the current architecture configuration if the direction indicator is in a decreased state; and

maintaining a state of the direction indicator for the selected instruction scheduler type.

15. (Withdrawn) The article of manufacture of claim 11, wherein adjusting comprises:

identifying a decrease in the effectiveness of the current architecture configuration;

identifying a direction indicator state for an instruction scheduler type of the current architecture configuration as one of an increased state and a decreased state;

reducing the number of active instruction schedulers for the current architecture configuration if the direction indicator is in an increased state;

increasing the number of active instruction schedulers for the current architecture configuration if the direction indicator is in a decreased state; and

switching a state of the direction indicator for the selected instruction scheduler type.

16. (Withdrawn) The article of manufacture of claim 15, wherein increasing the number of active instruction schedulers comprises:

selecting a disabled instruction scheduler of the current architecture configuration; and

enabling a clock input to the instruction scheduler and one or more associated functional blocks.

17. (Withdrawn) The article of manufacture of claim 15, wherein decreasing the number of active instruction schedulers comprises:

selecting an active instruction scheduler of the current architecture configuration; and

disabling a clock input to the instruction scheduler and one or more associated functional units.

18. (Original) The article of manufacture of claim 11, further comprising:

executing an adjusted architecture configuration over a predetermined interval;

computing an energy delay^2 product for the adjusted architecture configuration consumed during execution over the predetermined interval;

computing an energy delay^2 product for an increased architecture configuration having one or more additional active instruction schedulers than the adjusted configuration architecture consumed during execution over a reduced time interval;

computing an energy delay^2 product consumed by a decreased architecture configuration having a reduced number of active instruction schedulers than the adjusted configuration architecture consumed during over the reduced interval of time;

normalizing the computed energy delay^2 products for the increased and decreased architecture configurations;

identifying an architecture configuration having a lowest energy delay^2 product; and

selecting the identified architecture configuration as a current architecture configuration.

19. (Original) The article of manufacture of claim 18, further comprising:

detecting one of the increased architecture configuration or decreased architecture configuration as having the lowest energy delay^2 product;

performing the method of claim 18 with the detected architecture configuration as the adjusted architecture configuration.

20. (Original) The article of manufacture of claim 12, wherein computing the energy delay^2 product comprises:

calculating an energy consumption value for one or more functional units associated with the selected instruction scheduler;

calculating an energy consumption value for a register file associated with the selected instruction scheduler;

calculating an energy consumption value for each component of the selected instruction scheduler;

summing the energy consumption values of the instruction scheduler, functional units and the register file; and

computing the energy delay^2 product as a product of the energy consumption sum and a square of the predetermined time interval.

21. (Withdrawn) A clustered micro-architecture comprising:

a plurality of execution clusters, each execution cluster including at least one instruction scheduler;

a steering unit to assign a received instruction to an execution cluster; and

a resize circuit to adjust a number of active instruction schedulers of the micro-architecture according to an energy efficiency of a current architecture configuration.

22. (Withdrawn) The clustered micro-architecture of claim 21, wherein each execution cluster comprises:

enable/disable logic to activate/deactivate an instruction scheduler and one or more associated logic units of an execution cluster according to the resize circuit.

23. (Withdrawn) The clustered micro-architecture of claim 21, wherein each execution cluster further comprises:

a plurality of logic components to enable issuance of received instructions, each logic component comprising:

an activity counter to maintain an access count of the respective logic component during a time interval;

an energy per access register to contain an energy amount consumed by the respective logic component per access; and

an energy computation register to contain an energy consumption value as a product of the access count from the activity counter and the energy amount from the energy per access register,

wherein the resize circuit to select an energy consumption value from each energy computation register to compute an energy delay^2 product value for each instruction scheduler type as a product of a sum of the selected energy consumption values and the square of the time interval.

24. (Withdrawn) The clustered micro-architecture of claim 21, wherein the plurality of logic components comprises:

a register file;

a functional unit to execute the instruction; and

a data cache and data TLB for a memory instruction scheduler.

25. (Withdrawn) The clustered micro-architecture of claim 21, wherein the at least one instruction scheduler comprises:

a floating point instruction scheduler;

an integer instruction scheduler;

a memory instruction scheduler; and

a copy instruction scheduler.

26. (Withdrawn) A system comprising:

a self-contained power source;

a memory controller coupled to a memory; and

a processor coupled to the memory controller including:

a plurality of execution clusters, each execution cluster including at least one instruction scheduler,

a steering unit to assign a received instruction to an execution cluster, and

a resize circuit to adjust a number of active instruction schedulers of the micro-architecture according to an energy efficiency of a current architecture configuration.

27. (Withdrawn) The system of claim 26, wherein each execution cluster comprises:

enable/disable logic to activate/deactivate an instruction scheduler of an execution cluster according to the resize circuit.

28. (Withdrawn) The system of claim 26, wherein each execution cluster further comprises:

a plurality of logic components to enable issuance of received instructions, each logic component comprising:

an activity counter to maintain an access count of the respective logic component during a time interval;

an energy per access register to contain an energy amount consumed by the respective logic component per access; and

an energy computation register to contain an energy consumption value as a product of the access count from the activity counter and the energy amount from the energy per access register,

wherein the resize circuit to select an energy consumption value from each consumed energy register to compute an energy delay^2 product value for each instruction scheduler type as a product of a sum of the selected energy consumption values and the square of the time interval.

29. (Withdrawn) The system of claim 26, wherein the at least one instruction scheduler comprises:

a floating point instruction scheduler;

an integer instruction scheduler;

a memory instruction scheduler; and

a copy instruction scheduler.

30. (Withdrawn) The system of claim 26, further comprising:

an input/output controller coupled to the I/O controller.